Xilinx WebPACK 9.2i On DICE

Archie Howitt

This mornings talk will cover

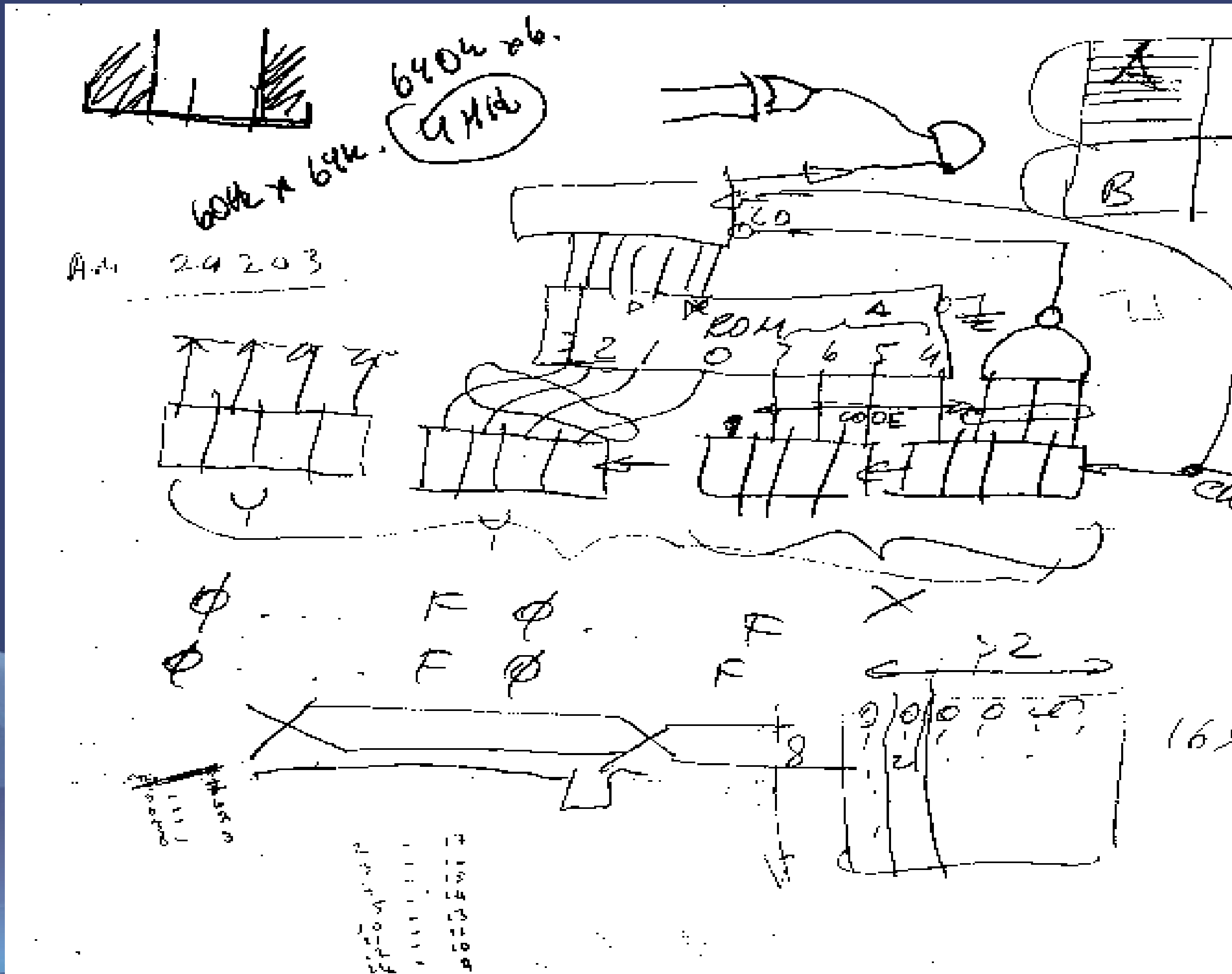
- Historical background
- Implementing WebPACK 9.2i on DICE
- Xilinx ISE
- What is Verilog

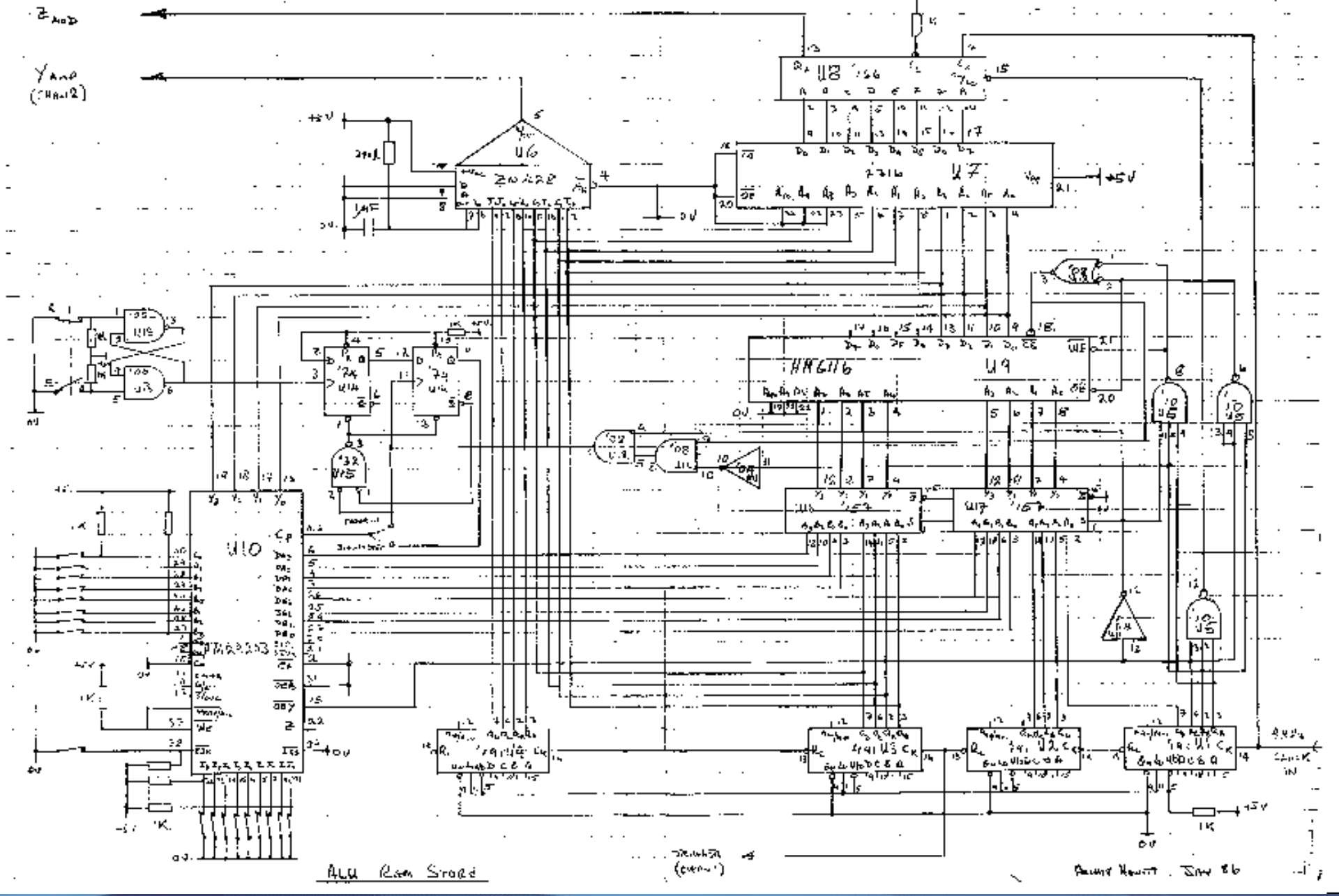
Acknowledgments

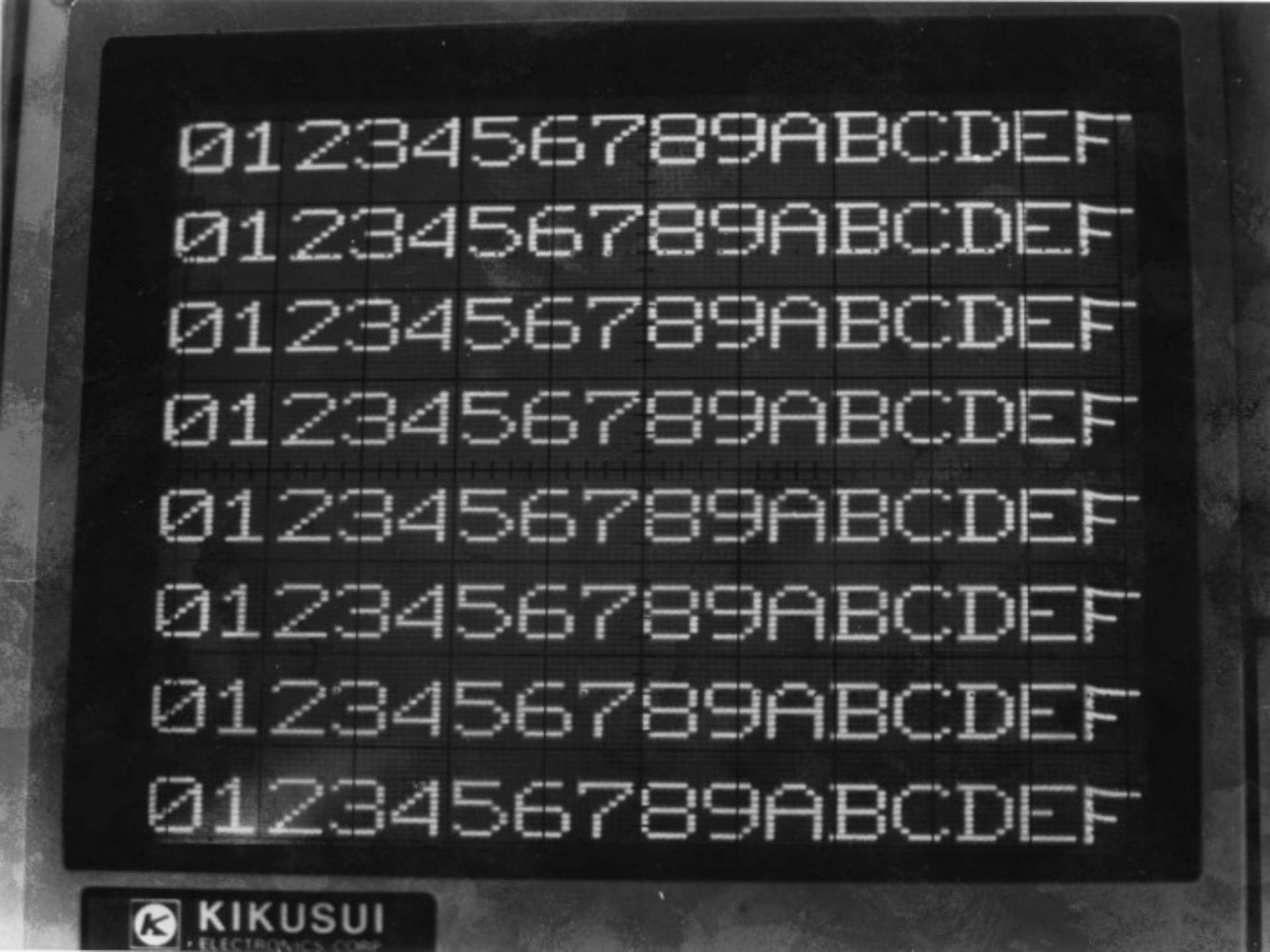
- Xilinx - Scott Leishman
- SL5 kernel - Alastair Scobie
- General hand holding - Tim Colles

Historical Background

- Computer Design Labs 1985 – 2007
  - Initial remit – Sept 1985
  - Wiring complexity
  - Programmable logic
    - Altera Complex Logic device (CPLD)
    - Microchip PICs
  - Circuit Simulation & Synthesis
    - HASE simulator
    - Xilinx ISE


64K x 64K.
640K x6.
4 MHz
ROM
CODE
A
B


U8
U7
U9
U10
U6
HM6116
ALU Ram Stage


0123456789ABCDEF
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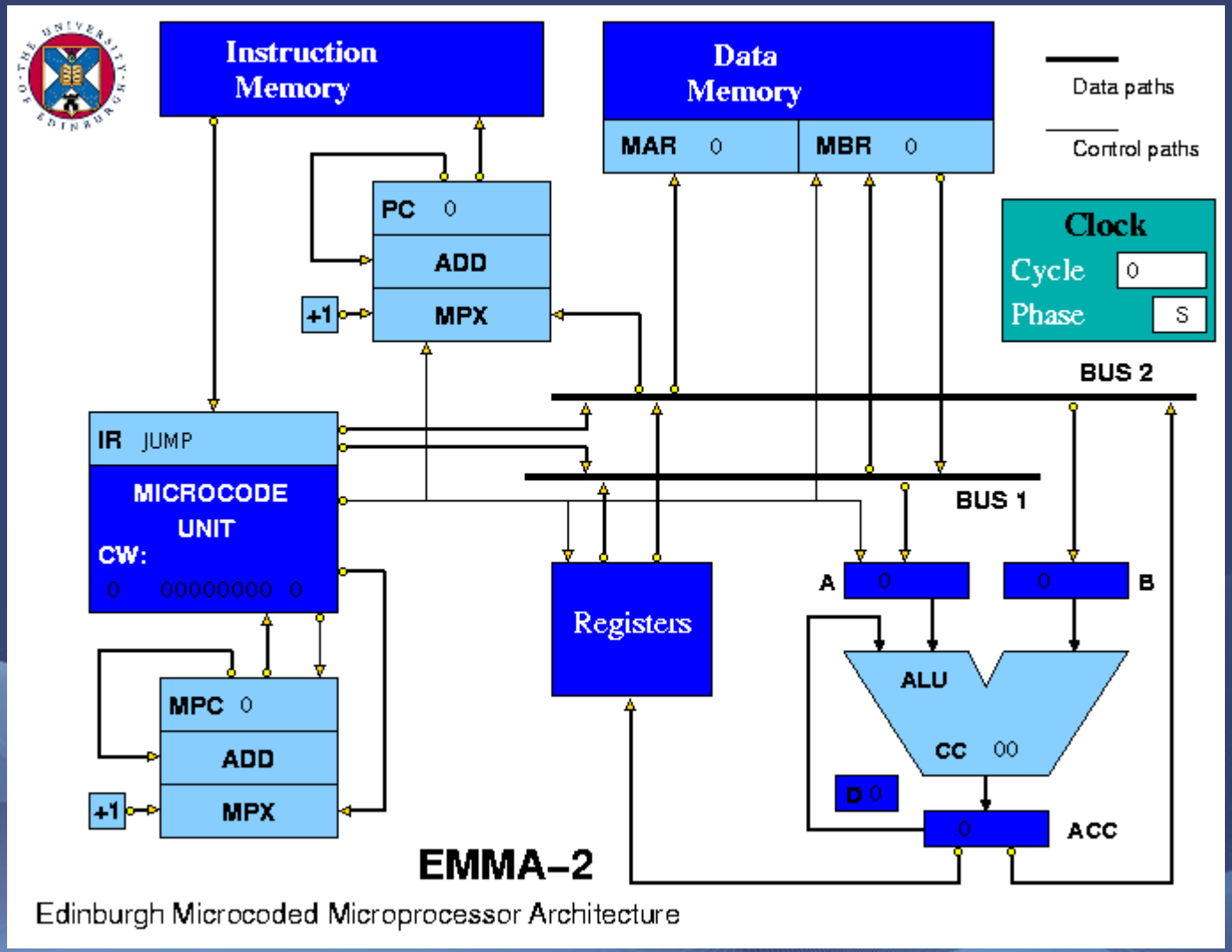
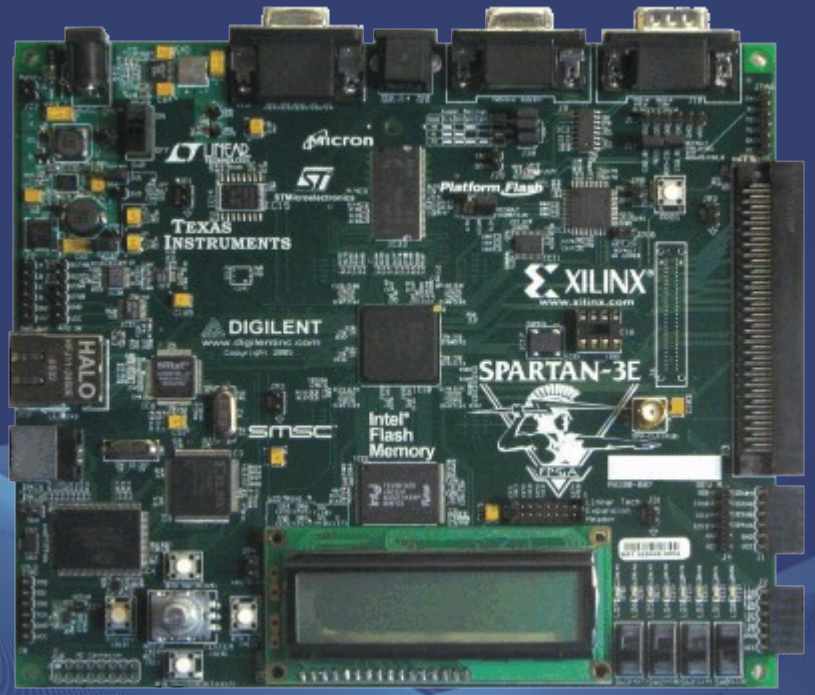
KIKUSUI

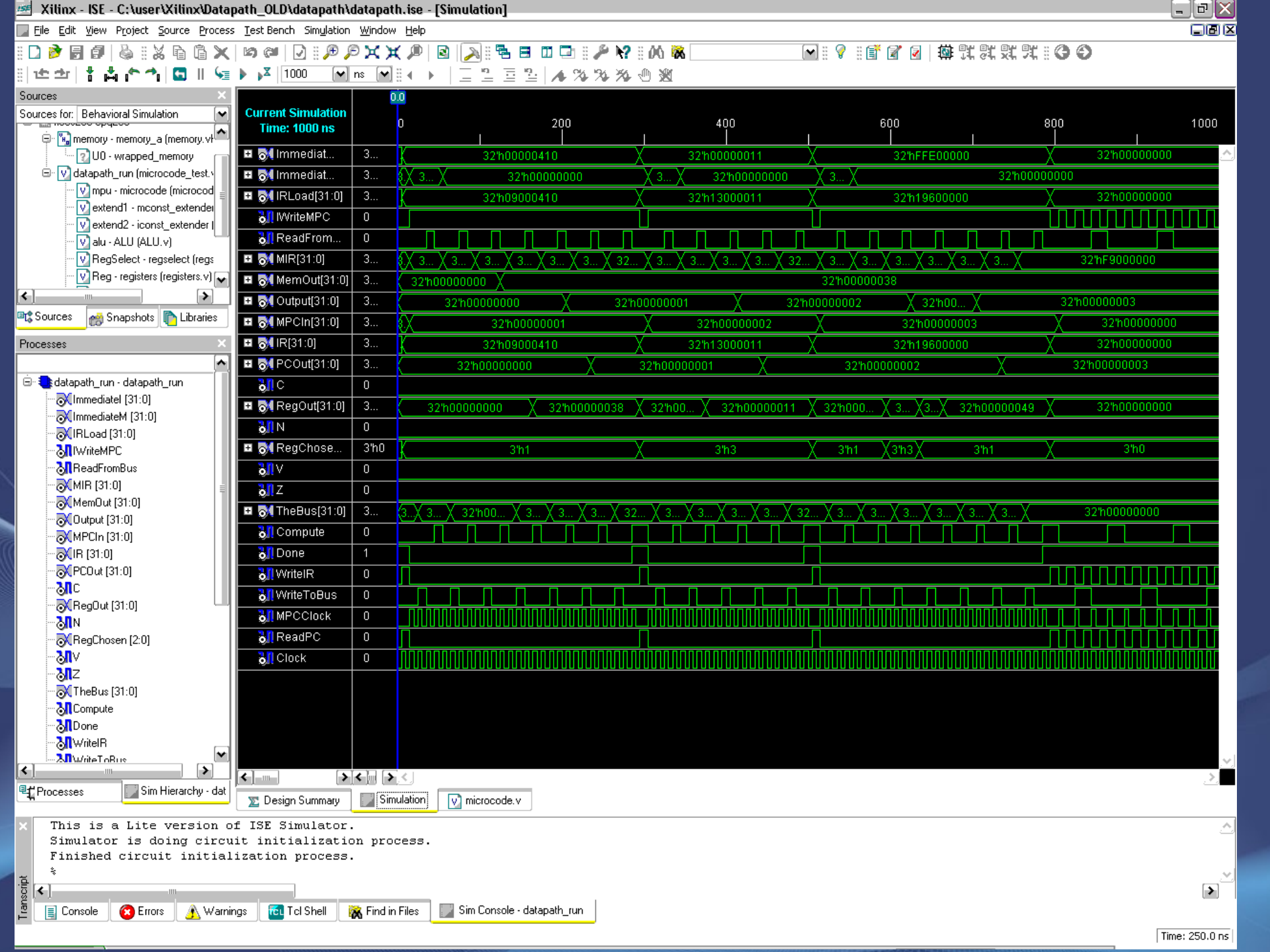

Instruction Memory
Data Memory
MAR 0
MBR 0
Data paths
Control paths
PC 0
ADD
+1
MPX
Clock
Cycle 0
Phase S
BUS 2
IR JUMP
MICROCODE UNIT
CW:
0 00000000 0
BUS 1
Registers
A 0
0 B
ALU
CC 00
D 0
0 ACC
MPC 0
ADD
+1
MPX
EMMA–2
Edinburgh Microcoded Microprocessor Architecture

Historical Background

Spartan-3



Spartan-3E


Xilinx - ISE - C:\user\Xilinx\Datapath_OLD\datapath\datapath.ise - [Simulation]
File Edit View Project Source Process Test Bench Simulation Window Help
Sources
Sources for: Behavioral Simulation
memory - memory_a (memory.vf
U0 - wrapped_memory
datapath_run (microcode_test.v
mpu - microcode (microcod
extend1 - mconst_extender
extend2 - iconst_extender
alu - ALU (ALU.v)
RegSelect - regselect (regs
Reg - registers (registers.v)
Sources
Snapshots
Libraries
Processes
datapath_run - datapath_run
Immediatel [31:0]
ImmediateM [31:0]
IRLoad [31:0]
IWriteMPC
ReadFromBus
MIR [31:0]
MemOut [31:0]
Output [31:0]
MPCIn [31:0]
IR [31:0]
PCOut [31:0]
C
RegOut [31:0]
N
RegChosen [2:0]
V
Z
TheBus [31:0]
Compute
Done
WriteIR
Processes
Sim Hierarchy - dat
Current Simulation Time: 1000 ns
0.0
0
200
400
600
800
1000
Immediat... 3... 32'h00000410 32'h00000011 32'hFFE00000 32'h00000000
Immediat... 3... 3... 32'h00000000 3... 32'h00000000 3... 32'h00000000
IRLoad[31:0] 3... 32'h09000410 32'h13000011 32'h19600000 32'h00000000
IWriteMPC 0
ReadFrom... 0
MIR[31:0] 3... 32'hF9000000
MemOut[31:0] 3... 32'h00000000 32'h00000038
Output[31:0] 3... 32'h00000000 32'h00000001 32'h00000002 32'h00... 32'h00000003
MPCIn[31:0] 3... 32'h00000001 32'h00000002 32'h00000003 32'h00000000
IR[31:0] 3... 32'h09000410 32'h13000011 32'h19600000 32'h00000000
PCOut[31:0] 3... 32'h00000000 32'h00000001 32'h00000002 32'h00000003
C 0
RegOut[31:0] 3... 32'h00000000 32'h00000038 32'h00... 32'h00000011 32'h000... 3... 3... 32'h00000049 32'h00000000
N 0
RegChose... 3'h0 3'h1 3'h3 3'h1 3'h3 3'h1 3'h0
V 0
Z 0
TheBus[31:0] 3... 32'h00000000
Compute 0
Done 1
WriteIR 0
WriteToBus 0
MPCClock 0
ReadPC 0
Clock 0
Design Summary
Simulation
microcode.v
This is a Lite version of ISE Simulator.
Simulator is doing circuit initialization process.
Finished circuit initialization process.
%
Transcript
Console
Errors
Warnings
Tcl Shell
Find in Files
Sim Console - datapath_run
Time: 250.0 ns

Implementing WebPACK 9.2i On DICE

- What is WebPACK?
  - Integrated Software Environment - ISE
  - Install Drivers
- Problems
  - WebPACK supported on Enterprise Linux only
  - Install Drivers requires kernel modules
  - Compatibility problems with FC6

Implementing WebPACK 9.2i On DICE

- Solution
  - Scientific Linux 5
- Implementing on DICE
  - Maintain the FC6 DICE environment
  - Provide an SL5 kernel
  - Header files for lab machine installs

Implementing WebPACK 9.2i On DICE

- Lab machine profile

```
/*wizard*/

#include <dice/os/fc6.h>
#include <dice/hw/dell_optiplex_gx620.h>
#include <dice/options/studentlabs-at.h>
#include <dice/options/computerdesign.h>
#include <live/wire_h.h>

!profile.release      mSET(develop)

dhclient.mac 00:13:72:CF:6F:FB

/* Inventory information */

inv.sno          GH10C2J
inv.location     AT-3.09

/* End of file */
```

Implementing WebPACK 9.2i On DICE

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/* End of file */
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/* Defaults for CS3 Computer Design student lab machines in AT */

#include <dice/options/sl5kernel.h>

/* Packages required for piklab */
!profile.packages       mADD(piklab-0.14.2-2.fc6)
!profile.packages       mADD(pikdev-0.9.2-2.fc6)
!profile.packages       mADD(pikloops-0.2.1-6.fc6)
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!profile.packages       mADD(gputils-0.13.4-2.fc6)
!profile.packages       mADD(gpsim-0.22.0-2.fc6)
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/* packages required for xilinx */
!profile.packages               mADD(fxload-2002_04_11-1.fc6.ccrma)

/* Wrapper and driver required for Xilinx WebPACK ISE */
!profile.packages               mADD(xilinx-ise-wrapper-92i-0.dice.3)
!profile.packages               mADD(xilinxdrivers-92i-0.dice.1)

/* Load xilinx usb drivers modules on startup */
!boot.services                  mADD(rc_xilinx)

/* we need openmotif (from SL5) for pace but clashes with aclisp */
!profile.packages               mADD(openmotif-2.3.0-0.3.el5)
!profile.packages               mADD(openmotif-devel-2.3.0-0.3.el5)
!profile.packages               mADD(-aclisp-*-*)
!profile.packages               mADD(-lkb-*-*)
!LCFG_UPDATE.rpmpath    mCONCAT(_REPOSITORY)
!LCFG_UPDATE.rpmpath    mCONCATQ("/sl5/distro,")
!file.files                     mADD(libxm)
file.file_libxm                 /usr/lib/libXm.so.3
file.type_libxm                 link : zap
file.tmpl_libxm                 /usr/lib/libXm.so.4

/* Label these machines on profile page as Computer Design */
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/* eof */
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```

```
#ifndef DICE_OPTIONS_SL5KERNEL
#define DICE_OPTIONS_SL5KERNEL

#include <lcfg/options/sl5kernel.h>

#endif
```

```
/* Option header to use SL5 kernel
                                        */

#ifndef LCFG_OPTIONS_SL5KERNEL
#define LCFG_OPTIONS_SL5KERNEL

/* This is a temporary option header until someone works out how
   to do this properly */

#ifdef LINUX_FC6
!profile.packages          mADD(sl5kernel)
profile.packages_sl5kernel      +kernel-2.6.18-8.1.6.el5inf/i686 \
                          +kernel-headers-2.6.18-8.1.6.el5inf \
                          +kernel-devel-2.6.18-8.1.6.el5inf/i686 \
                          +openafs-kernel-1.4.4-2.6.18_8.1.6.el5inf_2/i686
#endif LINUX_FC6

#endif


/* EOF */
```

```
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- Let's look at the SPEC files for:
  - xilinx-ise- wrapper-92i-0.dice.3
  - xilinxdrivers-92i-0.dice.1

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!profile.packages               mADD(-aclisp-*-*)
!profile.packages               mADD(-lkb-*-*)
!LCFG_UPDATE.rpmpath    mCONCAT(_REPOSITORY)
!LCFG_UPDATE.rpmpath    mCONCATQ("/sl5/distro,")
!file.files                     mADD(libxm)
file.file_libxm                 /usr/lib/libXm.so.3
file.type_libxm                 link : zap
file.tmpl_libxm                 /usr/lib/libXm.so.4

/* Label these machines on profile page as Computer Design */
!profile.comment        mADD( - Computer Design)

/* eof */
```

Xilinx ISE

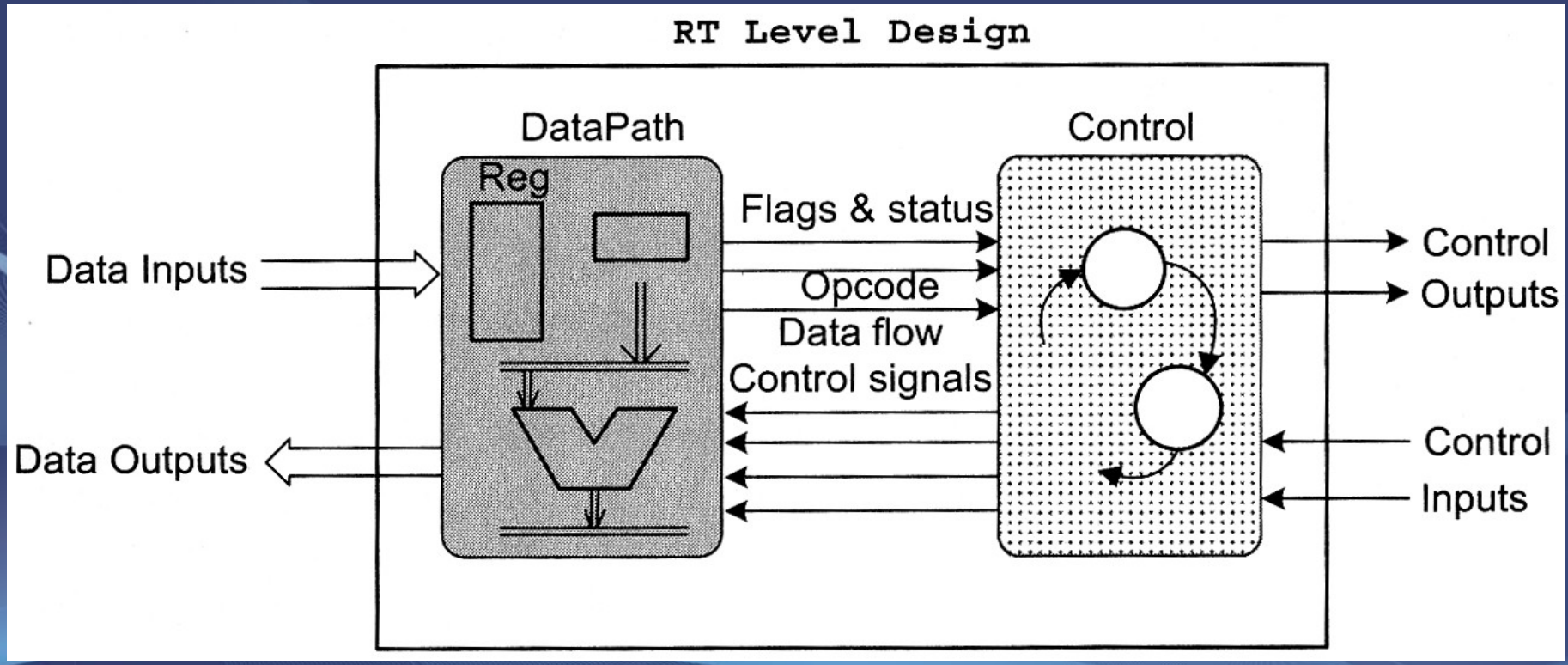
- ISE Demonstration
  - Implement an XOR gate
  - Program the Spartan-3E Board

What is Verilog

- Verilog Hardware Description Language (Verilog HDL)
  - IEEE Std 136-2001
  - Register Transfer Level (RTL)
    - Simulation
    - Synthesis
    - Testbench Generation
    - Verification Tools
- Quick Overview
  - Let's see if we can make a Multiplexer

What is Verilog

- Control/data Partitioning
  - The first step in RTL design is partitioning into data and control parts



What is Verilog

```
module DataPath
        (DataInput, DataOutput, Flags, Opcodes, ControlSignals);

        input    [15:0] DataInputs;
        output   [15:0] DataOutputs;
        output   Flags;
        output   Opcodes;
        input    ControlSignals;
        // instantation of data components
        // ...
        // interconnection of data components
        // bussing specification

endmodule
```

What is Verilog

```
module DataComponent (DataIn, DataOut, ControlSignals);

        input     [7:0] DataIn;
        output    [7:0] DataOut;
        input     ControlSignals;
        // Depending onControlSignals
        // operate on DataIn and
        // produce DataOut

endmodule
```

What is Verilog

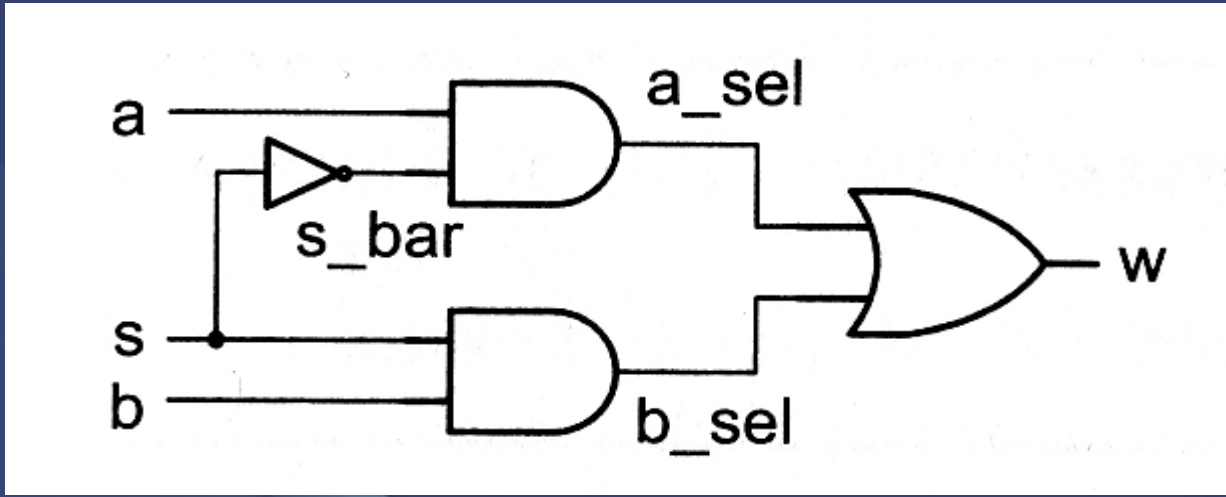
```
module ControlUnit (Flags, Opcodes, ExternalControls, ControlSignals);

        input     Flags;
        input     Opcodes;
        input     ExternalControls;
        output    ControlSignals;
        // Based on inputs decide what
        // control signals to issue
        // and what next state to take

endmodule
```

What is Verilog

- Primitive instantiation of our multiplexer




```
module MultiplexerA (input a, b. s output w);
    wire    a_sel, b_sel, s_bar;
    not     U1 (s_bar, s);
    and     U2 (a_sel, a, s_bar);
    and     U3 (b_sel, b, s);
    or      U3 (w, a_sel, b_sel);
endmodule
```

What is Verilog

- Boolean expressions describing our multiplexer

```
module MultiplexerB (input a, b, s, output w);
      assign   w = (a & ~s) | (b & s);
endmodule
```

What is Verilog

- Multiplexer using Conditional Expression

```
module MultiplexerC (input a, b, s, output w);
      assign   w = s ? b : a;
endmodule
```

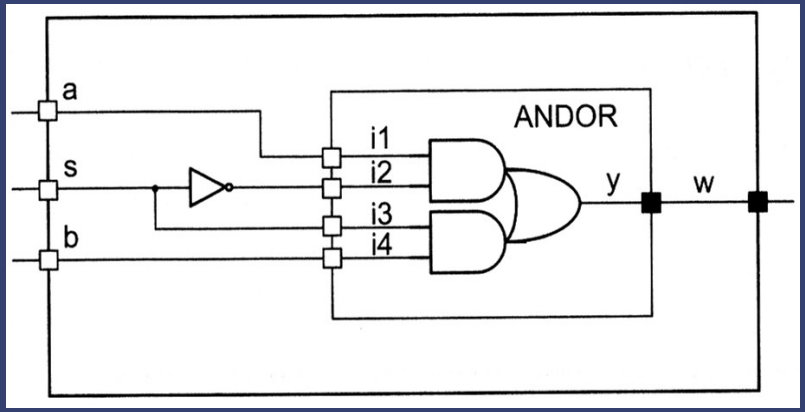
What is Verilog

- Procedural blocks or constructs for our complex multiplexer

```
module MultiplexerD (input a, b, s, output w);
    reg      w;
    always   @ (a, b, s) begin
             if (s) w = b;
             else w = a;
    end
endmodule
```

What is Verilog

- Module Instantiations




```
module ANDOR (input i1, i2, i3,i 4, output y);
      assign y = (i1 & i2) | (i3 & i4);
endmodule

module MultiplexerE (input a, b, s, output w);
      wire      s_bar;
      not       U1 (s_bar, s);
      ANDOR U3 (a, s_bar, s, b, w);
endmodule
```

What is Verilog

- Octal 2-to-1 Multiplexer

```
`timescale 1ns/100ps
module Mux8 (input sel, input [7:0] data1, data0,
                                        output [7:0] bus1);
    assign #6 bus1 = sel ? data1 : data0;
endmdule
```

The End